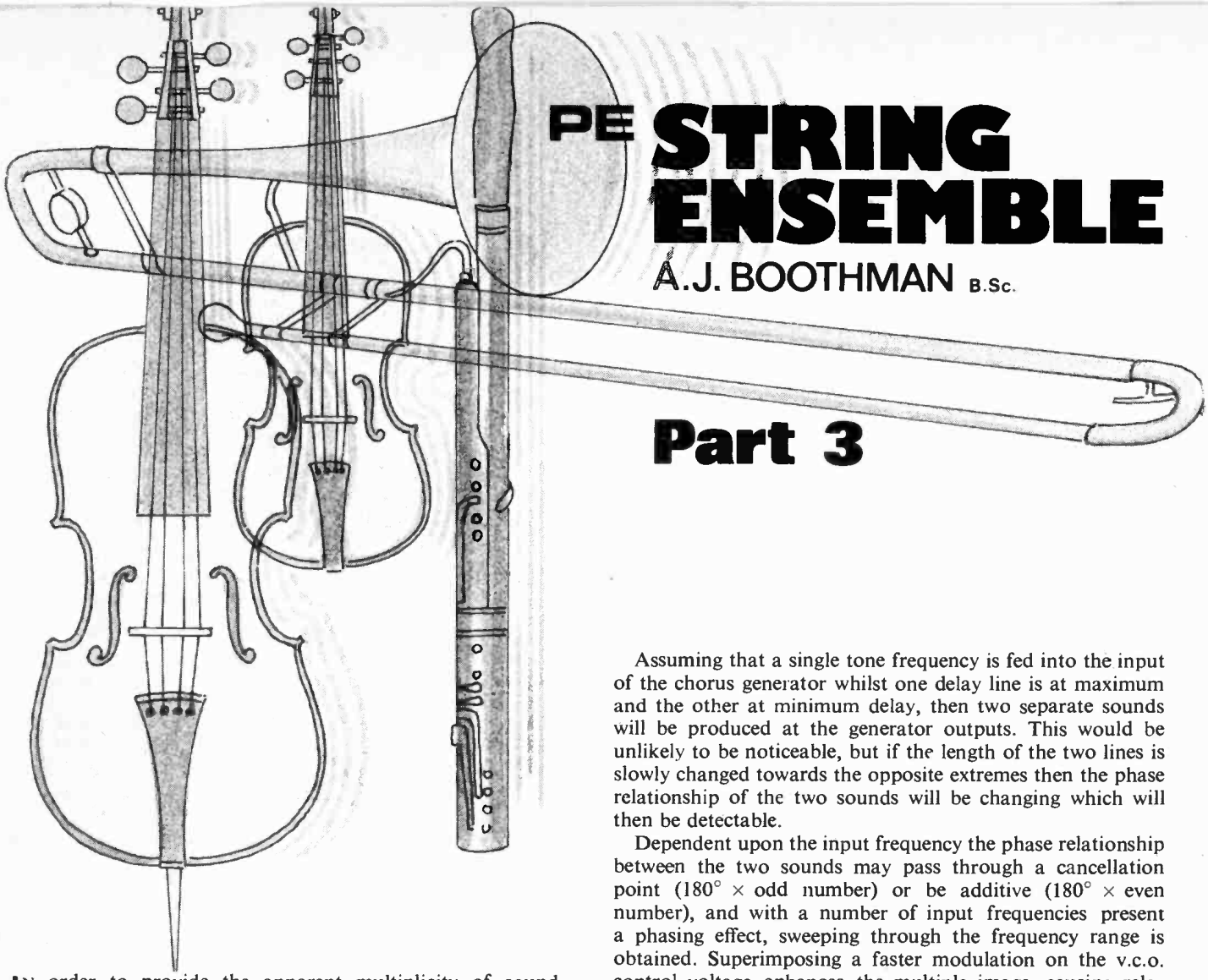

# PE STRING ENSEMBLE

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## Part 3

IN order to provide the apparent multiplicity of sound sources, producing similarly pitched notes, required to simulate the orchestral string section effect, a Chorus Generation System is described which relies on the use of bucket brigade analogue delay lines for its fundamental operation.

### CHORUS GENERATION SYSTEM

The system is shown in block schematic form in Figure 3.1. For reasons described later the input is processed by a low pass filter thus reducing the maximum frequency fed into the delay lines. Two active low pass filters follow each of the delay lines to complete the signal paths, extracting the clock frequency break through, and reconstituting the sampled waveform.

The two-phase clock circuits produce square waves in anti-phase from v.c.o.s A and B (see inset example of waveforms associated with Delay Line A), and both v.c.o.s are controlled in frequency by the combination of slow and fast modulator outputs which have been amplified to a suitable drive level. The two v.c.o.s work in an opposing manner in that as the control voltage increases, the frequency for one v.c.o. increases whilst the frequency for the other v.c.o. decreases, and vice versa.

Since the delay in each line is inversely proportional to the clock frequency, the delay in one line reduces whilst the delay in the second line increases and vice versa. When the control voltage is in the mid position the two delay lines have equal delays of approximately 3·5ms, varying between approximately 2·5ms and 5ms at the extremes.

Assuming that a single tone frequency is fed into the input of the chorus generator whilst one delay line is at maximum and the other at minimum delay, then two separate sounds will be produced at the generator outputs. This would be unlikely to be noticeable, but if the length of the two lines is slowly changed towards the opposite extremes then the phase relationship of the two sounds will be changing which will then be detectable.

Dependent upon the input frequency the phase relationship between the two sounds may pass through a cancellation point (180° × odd number) or be additive (180° × even number), and with a number of input frequencies present a phasing effect, sweeping through the frequency range is obtained. Superimposing a faster modulation on the v.c.o. control voltage enhances the multiple image, causing relatively rapid changes in phase relationship which when combined with the slow sweep give a complex pattern of relative phase simulating more than two sources and resulting in a rich chorus sound. The sweep rates of the slow and fast modulators are approximately 0·5Hz and 10Hz respectively.

### BUCKET BRIGADE

The term "Bucket Brigade Delay Line", is derived from the anology of a number of people, each with a bucket, forming a chain along which it is desired to transmit water.

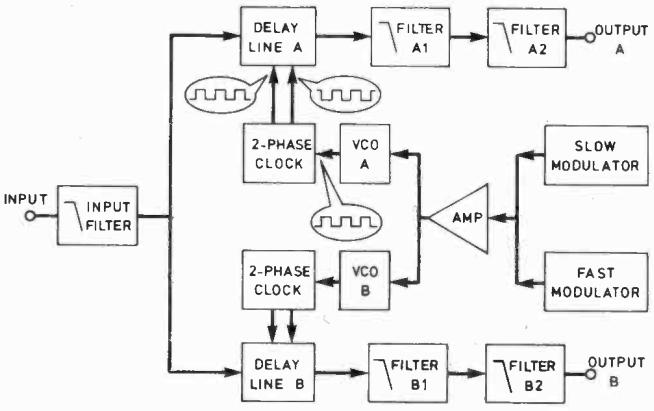


**Fig. 3.1. Schematic of Chorus Generation system**

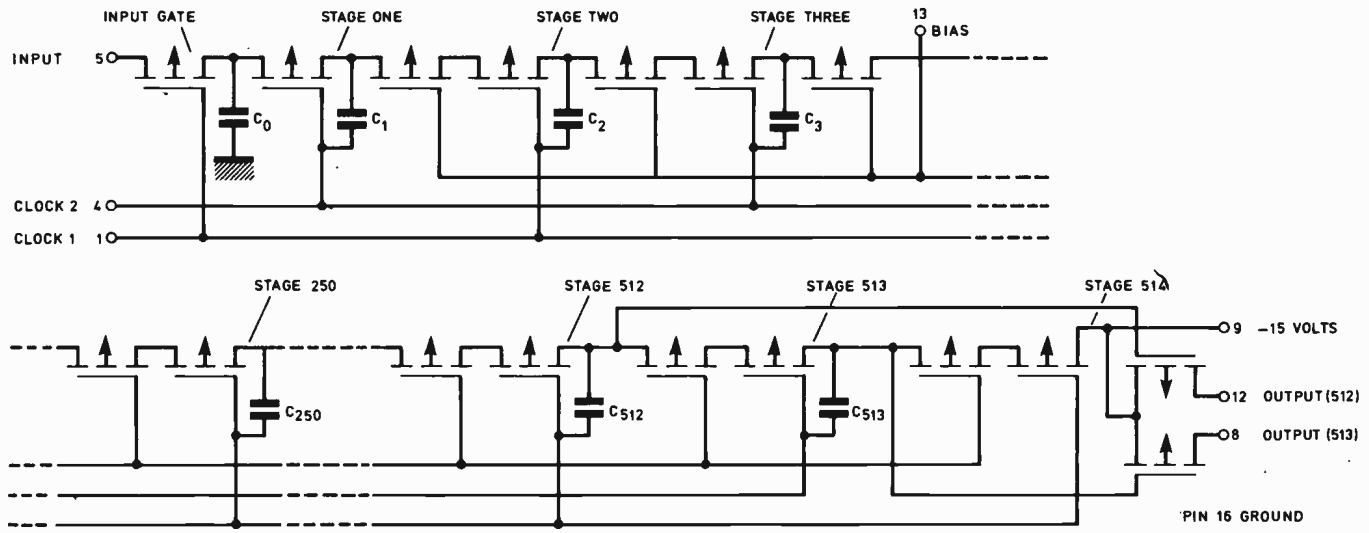


**Fig. 3.2. Circuit of TDA1022 analogue delay line**

Assuming that the first person has a full bucket, and all others are empty, it is possible to pour the water from bucket one into bucket two, then bucket two into bucket three, and so on until eventually all the water from the first bucket, excluding spillage, is transferred to the last bucket.

This description infers a delay which is dependent on both the speed at which each person reacts in filling his neighbour's bucket, and the number of buckets in the chain. In the String Ensemble it is fundamental that this delay line is controllable at will, and since the number of buckets, or stages in the device, is constant it is necessary to instruct each person how quickly to react before pouring the contents of their bucket into the next bucket, thus controlling the overall delay. The reaction time is quoted since in the electronic version the speed of pouring is very high such that variation in the "stage delay" is controlled by introducing a pause before the instruction to pour. Electronically the pause is created by an instruction to pour constituting the leading edge of a square wave which is known as the "clock". An increase in clock frequency corresponds to shouting "pour" at greater frequency thus shortening the stage and overall delay.

Carrying the analogy further, two instructions are used, which equate to two clocks, where one can visualise one male and one female instructor each instructing persons of their own sex in a line where the sexes are alternated. This is only a matter of electronic convenience and in future generations of bucket brigade delay line i.c.s one can expect that the required conversion from a single clock will be carried out in the same package.

## ANALOGUE DELAY

The system described above can be digital or analogue, in the first case either full or empty buckets would always be concerned and in the second case the amount of water in the last bucket would directly relate to the amount contained in the first bucket as it commenced its journey.

In order to fully understand the electronic analogue delay line, sometimes called the analogue shift register, an alternative method of operation within our chain of bucket carriers and water pourers should be considered. Since we are not concerned with the actual transfer of water along the chain, but simply require to know how much water was in the first bucket when the chain commenced its sequence of operation, we can start with all buckets full apart from the first one which will be filled to the amount (analogue) of interest. On the first instruction (leading edge of Clock 1) the first person (male) puts the required amount of water into his bucket, which is equivalent to the level of the input signal at that moment, and on the second instruction the second person (female) fills up the first bucket leaving her with the same quantity of water previously contained in the first bucket. On the next instruction the third person fills up the second bucket and this continues down the line until the last bucket contains the same quantity of water as was present in the first bucket at the commencement of the sequence.

This can of course be a continuous process such that whilst the third person is topping up the second bucket, the first person is correcting the quantity in his bucket to match the new analogue or signal level.

## BUCKET BRIGADE DEVICES

Many of the earliest instruments incorporating analogue delay line i.c.s used an ITT device, the TGA350, which contains 185 stages of delay in the package, but since that time Reticon, Matsuchita and Phillips (Signetics) have produced devices in various configurations ranging from a single 512 stage line in a package to 2 × 512 stage lines, tapped lines, and now rumours of considerably longer lines in a package. The potential application for A.D.L.s are numerous including echo, reverberation, double tracking, flanging and phasing, vibrato, chorus generation, speech delay matching in P.A., signal scrambling, time compression, pseudo-stereo, voice threshold switching and test equipment circuitry particularly associated with oscilloscope storage displays.

## THE CHORUS MODE

Circuits have been proposed in which chorus is achieved by mixing a direct signal with the output of one delay line and the output of a second line fed from the first, both lines using the same changing clock frequency, but for the greatest effect the outputs from two or more lines should be mixed using clock frequencies modulated in an out of phase relationship—e.g. 180° for two lines, 120° for three lines. In practice this poses a problem for dual packaged lines in that on-chip intermodulation occurs in the form of both audio frequency tones and high noise. It is therefore necessary to use a separate package for each line, although noise advantages can be gained by using parallel dual lines in each position providing only one clock frequency is fed to the package.

## FREQUENCY CONSIDERATIONS

The bucket brigade principle described earlier relies on sampling the input waveform at discrete moments in time, and since a bucket cannot be involved in both filling and emptying operations at the same time, Bucket 1 must wait for the transaction between Buckets 2 and 3 to be completed before it can again be involved with Bucket 2, and half the information from the input is automatically lost. This imposes a relationship between the bandwidth (DC to maximum input frequency) and the clock frequency, such that the input bandwidth should be limited to less than one-half of the clock frequency, and normally to less than one-third. The resulting sampled waveform at the output of the delay line requires heavy filtering to recover the original waveform and remove the clock frequency content.

### TDA1022

The internal circuitry of the Signetics A.D.L. is shown in Fig. 3.2, using MOS technology f.e.t.s to switch the charge in the required manner between capacitors at each stage. The supply required is a nominal –15 volts, and at the clock frequencies used in the Ensemble (50–100kHz), the average delay for the 512 stages totals approximately 3·5ms, and for a distortion level of less than ½ per cent the input level can slightly exceed 2V r.m.s., with a band width of 12–15kHz, and attenuation through a line will be typically 4dB.

Fig. 3.3(a)–(h) indicate the operation of the delay line in conjunction with Fig. 3.2. Clocks 1 and 2 are in anti-phase, odd number stages linked to Clock 2 and even number stages, together with the input gate, connected to Clock 1.

Taking a waveform as shown in Fig. 3.3(b), the voltage present whilst Clock 1 is up is transferred direct to $C_0$ in Fig. 3.2. When Clock 2 rises the charge in $C_0$ is topped up reducing the charge in C to that which was previously present on $C_0$. Thus in Fig. 3.3(c) the voltage on $C_0$ rises to V and in Fig. 3.3(d) the voltage at the output of Stage 1 falls to the value at the input immediately prior to the rise of Clock 2. This situation now prevails until Clock 1 rises again at which time C is topped up reducing the charge on $C_2$ to that which was previously on $C_1$.

With the rise of Clock 1 again $C_0$ continues to monitor the input voltage such that when Clock 2 rises again the new voltage level (second sample) at the input, immediately prior to the rise of Clock 2, is transferred to the output of Stage 1, whilst the voltage at the output of Stage 2, which is equal to the first sample, is transferred to the output of Stage 3.

Thus it can be seen that the time taken for each sample to move from one stage to the next is half a clock period, and input samples are taken once per clock cycle with the input blocked for one half of each clock cycle.

When stage 512 is reached, a further stage (513) is used to fill in the half of the clock cycle during which a sample has not been passed through the delay line giving the stepped waveform shown in Fig. 3.3(h) which is then filtered to reconstitute the input waveform.

## CHORUS GENERATOR CIRCUITRY

The complete circuit of the Chorus Generator is given in Fig. 3.4. The bandwidth of the incoming signal is first limited by the low pass filter associated with IC19, and parallel connections taken to Channels A and B incorporating TDA1022 delay lines IC25 and IC26 respectively. The delay lines in each channel are followed by two low pass active filters based on IC20 and IC21 in Channel A and IC22 and IC23 in Channel B.

Clock frequencies are generated in IC28 and IC30 for Channel A and IC29 and IC31 for Channel B using the conventional v.c.o. configuration based on the CMOS 4007. In Channel A the variable resistance with voltage of the *n*-channel f.e.t. (pins 3, 4 and 5) is used to control the frequency of the oscillator comprising two gates of IC28 by virtue of its effect on the value of R59 which in combination with C45 determines its frequency of operation.

Two gates within IC30 are used to shape the waveform and produce an inverted version for the second phase of the clock.

In Channel B the *p*-channel f.e.t. (pins 1, 2 and 3) is used to control the oscillator comprising two gates in IC29, such that for the same modulation waveforms as pin 3 of IC30 and IC31, the oscillators work in anti-phase with respect to frequency variation.

Some gate wastage occurs in IC28 and IC29 due to the necessity to provide good decoupling of clock frequencies between the two channels, without which clock intermodulation would occur leading to a high noise level and swept audio frequencies at the output of the delay lines.

The modulation signals at pin 3 of the 4007's are generated by IC27 and amplified by IC24. IC27 is connected as two oscillators, similar to the clock oscillation but without voltage control, one operating at approximately 0·5Hz and the other at approximately 10Hz.

Filters, consisting of R47, C36, R48 and C37 for the slow modulator and R52, C40, R53 and C41, provide smooth modulation waveforms the level of which is controlled by VR9 and VR10 for slow and fast modulations respectively.

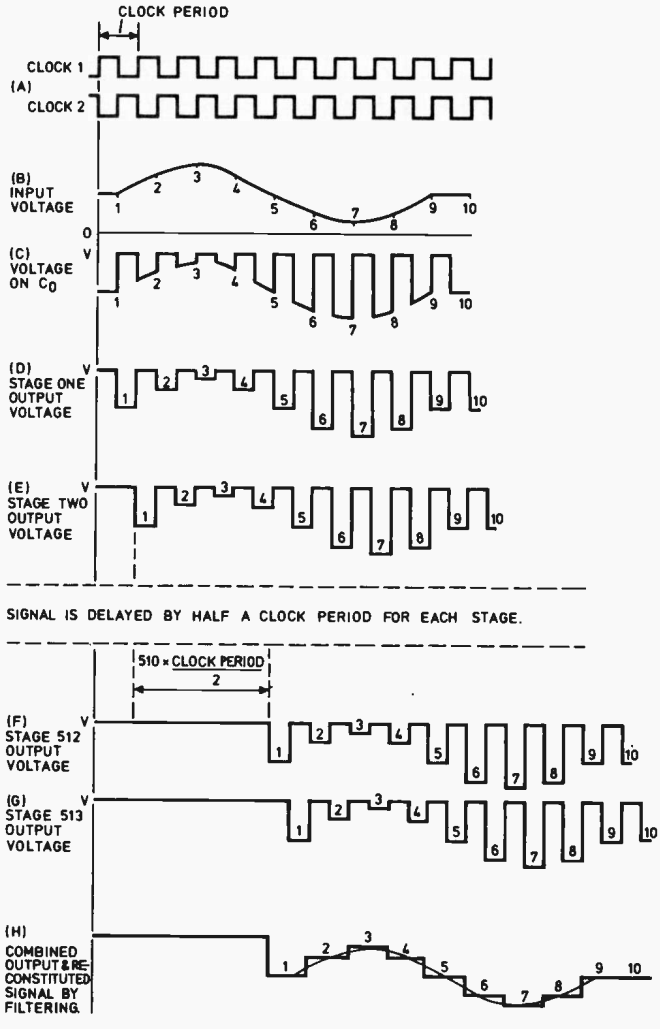


**Fig. 3.3. Waveshapes showing operation of delay line**

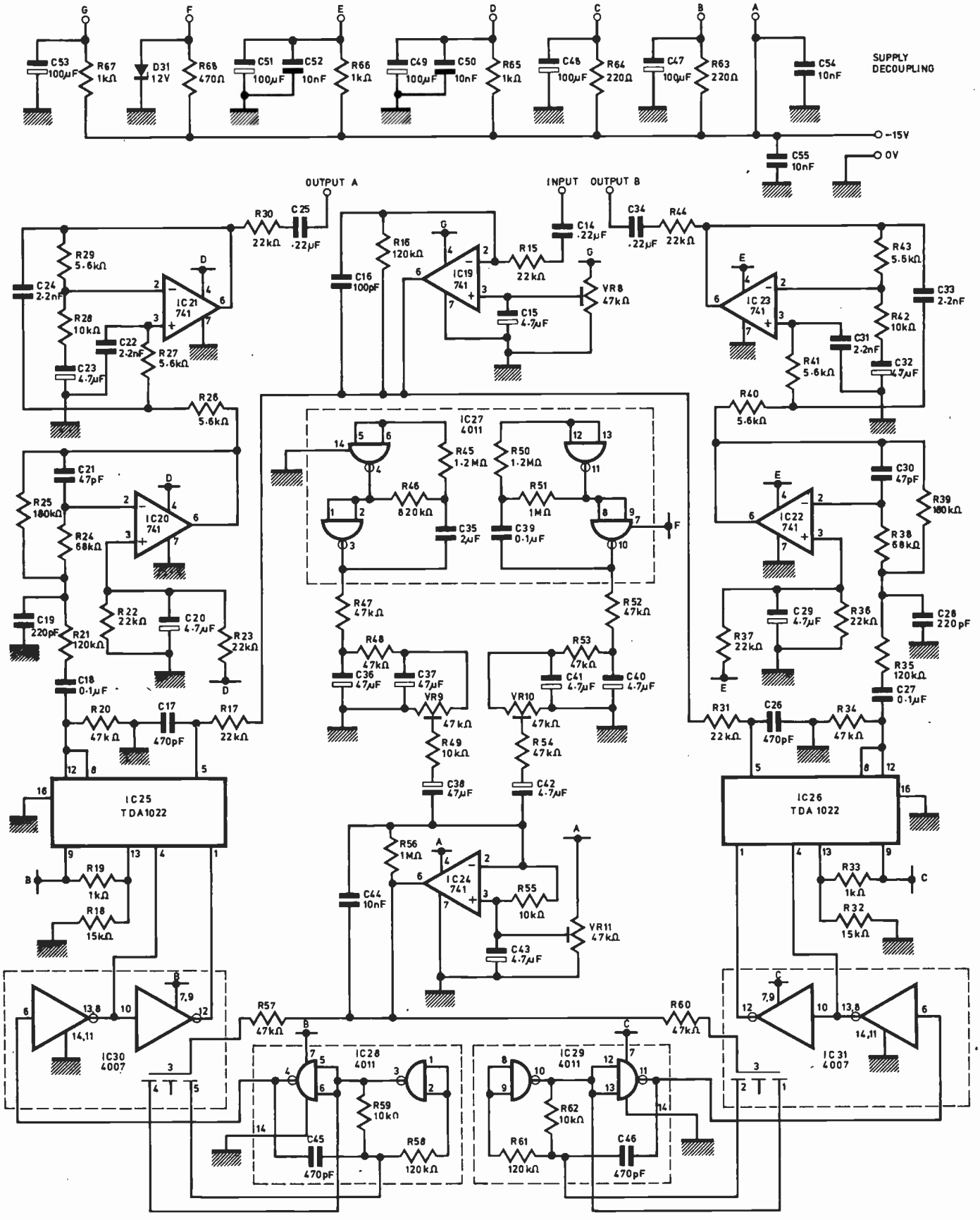


**Fig. 3.4. Circuit of Chorus Generator**

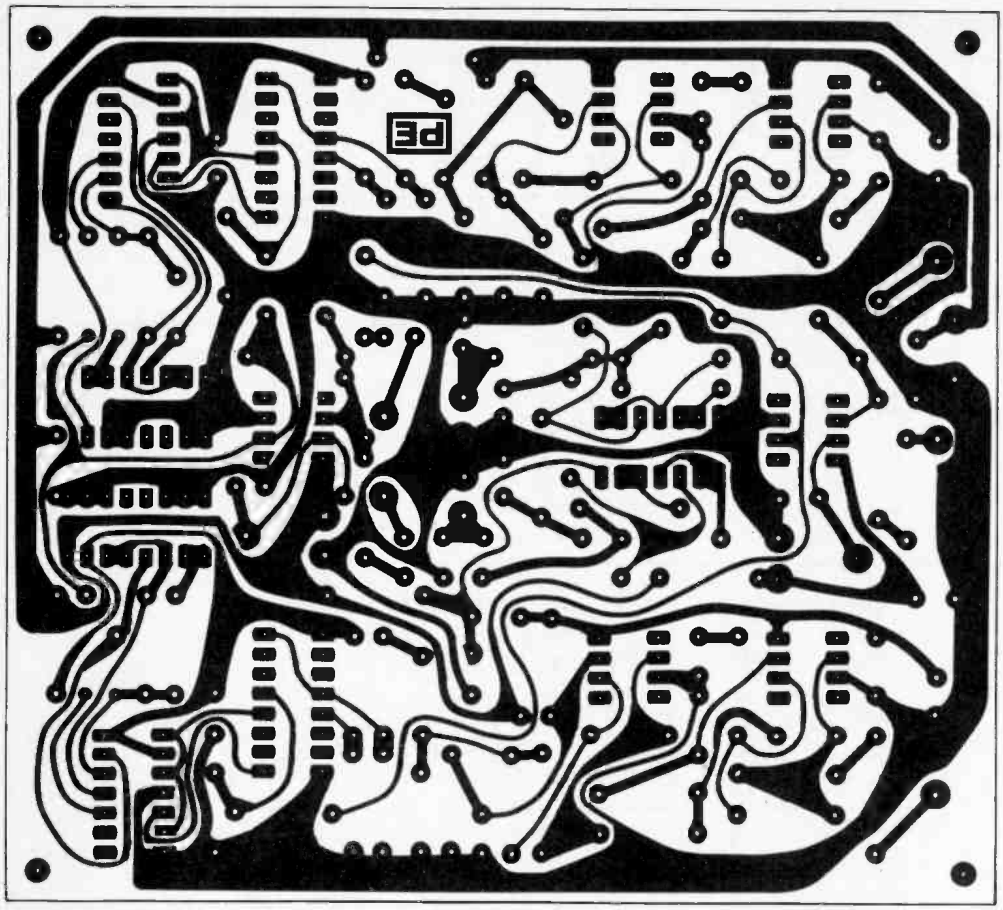

Fig. 3.5. Etching and drilling details of the Chorus Generation printed circuit board

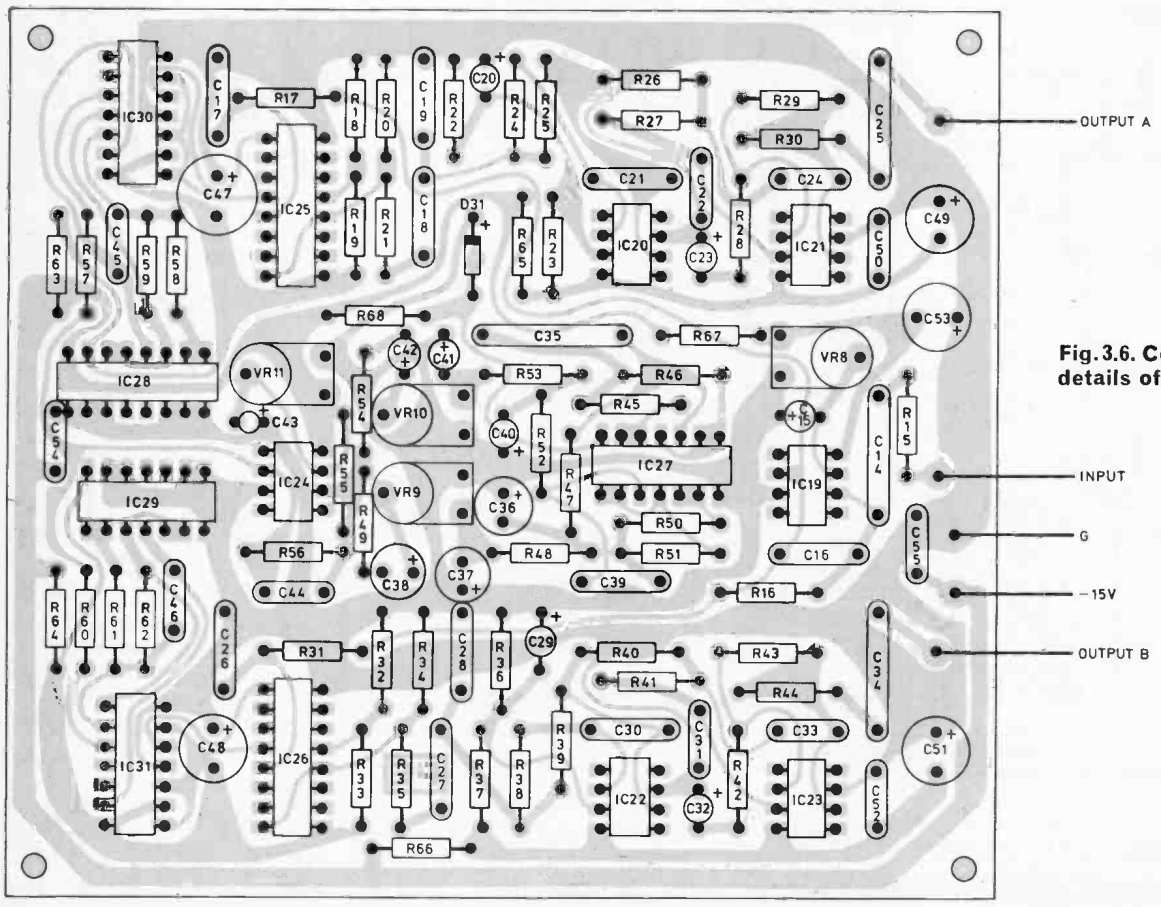


Fig. 3.6. Component assembly details of p.c.b.

## COMPONENTS . . .

### CHORUS GENERATOR

**Resistors**

| | | | | | |
|---|---|---|---|---|---|
| R15 | 22kΩ | R32 | 15kΩ | R49 | 10kΩ |
| R16 | 120kΩ | R33 | 1kΩ | R50 | 1·2MΩ |
| R17 | 22kΩ | R34 | 47kΩ | R51 | 1MΩ |
| R18 | 15kΩ | R35 | 120kΩ | R52–54 | 47kΩ |
| R19 | 1kΩ | R36–37 | 22kΩ | R55 | 10kΩ |
| R20 | 47kΩ | R38 | 68kΩ | R56 | 1MΩ |
| R21 | 120kΩ | R39 | 180kΩ | R57 | 47kΩ |
| R22–23 | 22kΩ | R40–41 | 5·6kΩ | R58 | 120kΩ |
| R24 | 68kΩ | R42 | 10kΩ | R59 | 10kΩ |
| R25 | 180kΩ | R43 | 5·6kΩ | R60 | 47kΩ |
| R26–27 | 5·6kΩ | R44 | 22kΩ | R61 | 120kΩ |
| R28 | 10kΩ | R45 | 1·2MΩ | R62 | 10kΩ |
| R29 | 5·6kΩ | R46 | 820kΩ | R63–64 | 220Ω |
| R30–31 | 22kΩ | R47–48 | 47kΩ | R65–67 | 1kΩ |
| ¼ watt 5% carbon film | | | | R68 | 470Ω |

**Capacitors**

| | |
|---|---|
| C14 | 0·22μF polyester |
| C15 | 4·7μF —V electrolytic |
| C16 | 100pF polystyrene |
| C17 | 470pF ceramic |
| C18 | 0·1μF polyester |
| C19 | 220pF polystyrene |
| C20 | 4·7μF 16V electrolytic |
| C21 | 47pF polystyrene |
| C22 | 2·2nF ceramic |
| C23 | 4·7μF 16V electrolytic |
| C24 | 2·2nF ceramic |
| C25 | 0·22μF polyester |
| C26 | 470pF ceramic |
| C27 | 0·1μF polyester |
| C28 | 220pF polystyrene |
| C29 | 4·7μF 16V electrolytic |
| C30 | 47pF polystyrene |
| C31 | 2·2nF ceramic |
| C32 | 4·7μF 16V electrolytic |
| C33 | 2·2nF ceramic |
| C34 | 0·22μF polyester |
| C35 | 2μF non polarised |
| C36–38 | 47μF 16V electrolytic |
| C39 | 0·1μF polyester |
| C40–43 | 4·7μF 16V electrolytic |
| C44 | 10nF ceramic |
| C45–46 | 470pF ceramic |
| C47–49 | 100μF 16V electrolytic |
| C50 | 10nF ceramic |
| C51 | 100μF 16V electrolytic |
| C52 | 10nF ceramic |
| C53 | 100μF 16V electrolytic |
| C54–55 | 10nF ceramic |

**Potentiometers**

VR8–11 47kΩ presets 100mW subminiature

**Diodes**

D31 12 volt 300mW Zener

**Integrated Circuits**

| | |
|---|---|
| IC19–24 | 741 |
| IC25–26 | TDA1022 |
| IC27–29 | 4011 |
| IC30–31 | 4007 |

**Miscellaneous**

1 Printed circuit board; 2–16 lead d.i.l. sockets; 5–14 lead d.i.l. sockets; 5 terminal pins

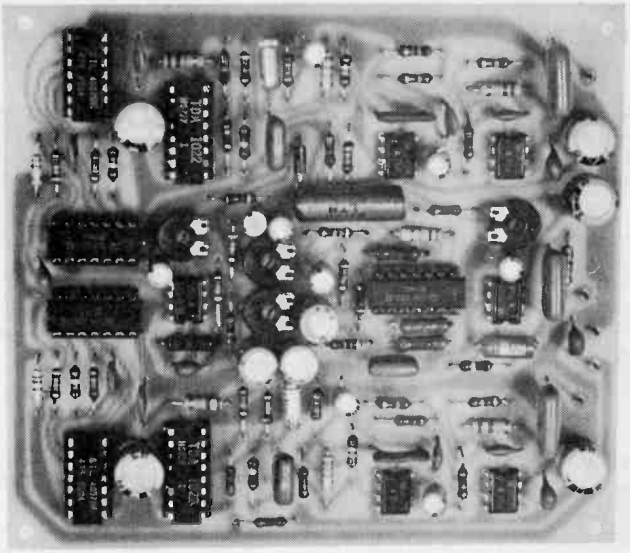

**Photo of Chorus Generation board**

### SETTING UP THE CHORUS GENERATOR

VR8 provides a d.c. control to the input filter which sets the input bias on both delay lines. This preset potentiometer should be adjusted such that with a signal present at the input, the combined A + B outputs will move from zero, through a distorted period, through a clear range, a further distorted period and back to zero. VR8 should be finally set for the centre of the clear transmission range to give maximum signal handling capacity for the delay lines.

With VR9 and VR10 at minimum, VR11 adjusts the centre frequency of the two v.c.o.s to approximately the same value. This is achieved by initially setting VR11 near its midpoint and VR9 slowly increased. The combined A and B output signals should be subject to a phasing effect with a smooth sweep and sweep turn-around characteristic. If the sweep appears to pause at one end, VR11 should be adjusted to recover the even sweep. VR9 should then be reduced and VR10 increased to mix in the fast modulator, the levels of both being adjusted to taste.

All the adjustments associated with the clock modulation are slow to take effect due to the long time constants associated with the slow modulator filters. This time constant also produces a turn on delay of a few seconds, before the chorus modulation commences, after switching on the instrument. Rapid adjustment will stop the chorus modulation which will then recover after a few seconds.

### CHORUS GENERATOR CONSTRUCTION

All the chorus generation circuits are mounted on a single printed circuit board, the etching and drilling details of which are given in Fig. 3.5 with the component assembly details in Fig. 3.6.

To assemble the board the previously recommended order of terminals, pins, resistors, Zener (D31), i.c. sockets, preset potentiometers, small capacitors, and finally large capacitors may be used. Sockets are recommended for the 14 and 16 lead i.c.s which are all of MOS type and therefore sensitive to handling, but these are not necessary for the 741 type i.c.s.

Careful attention should be paid to correct orientation of the i.c.s.

*Note—the track cutting amendment given finally last month refers to IC3*

**NEXT MONTH: Voice/preamp board construction**